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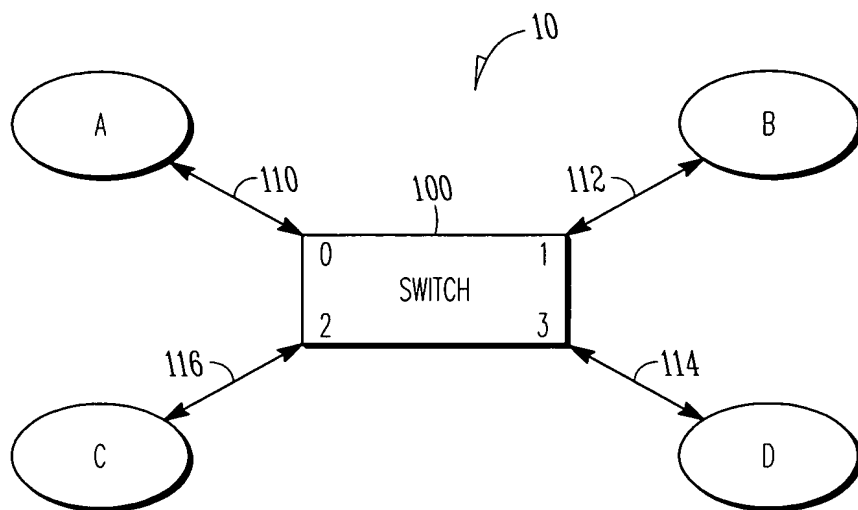


FIG. 1

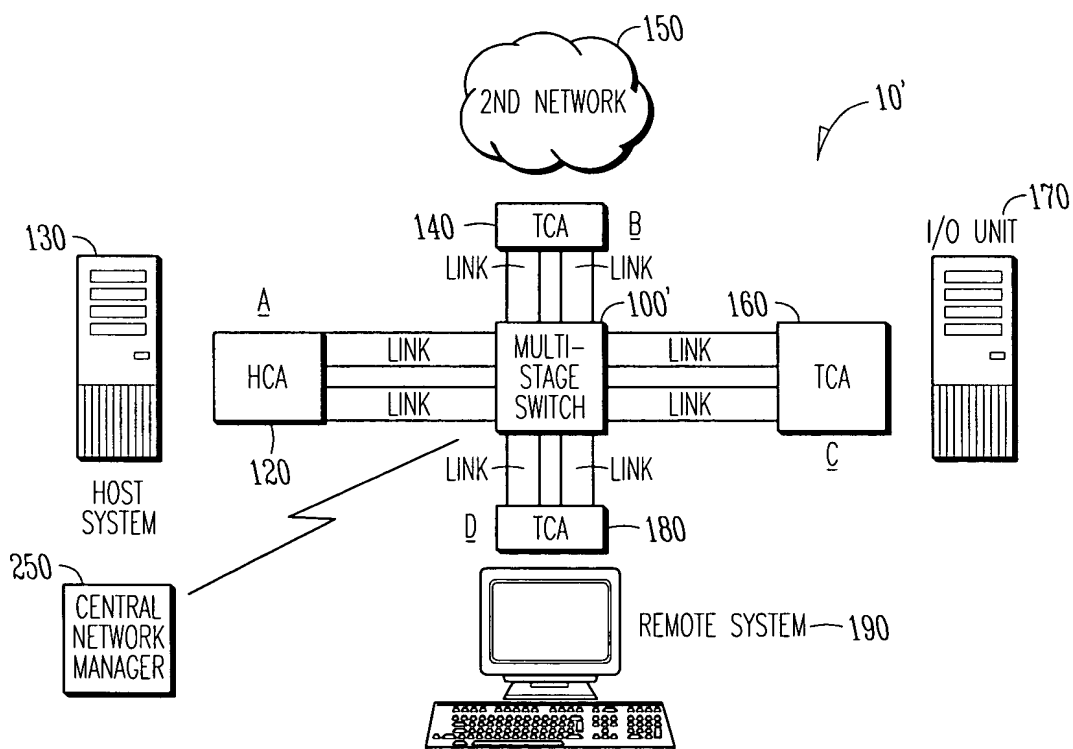


FIG. 2

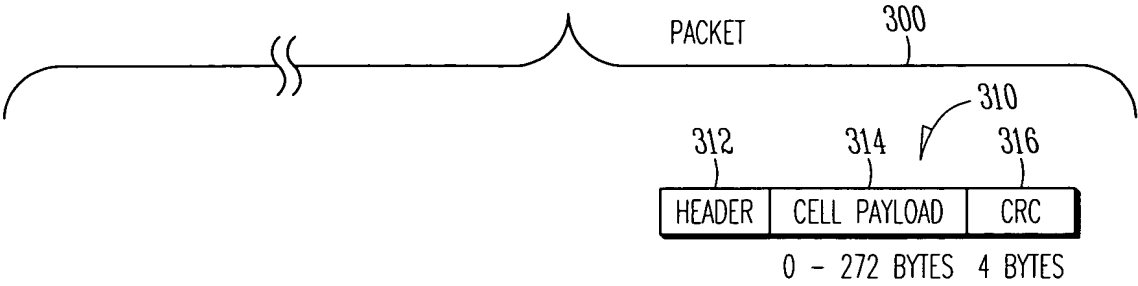


FIG. 3A

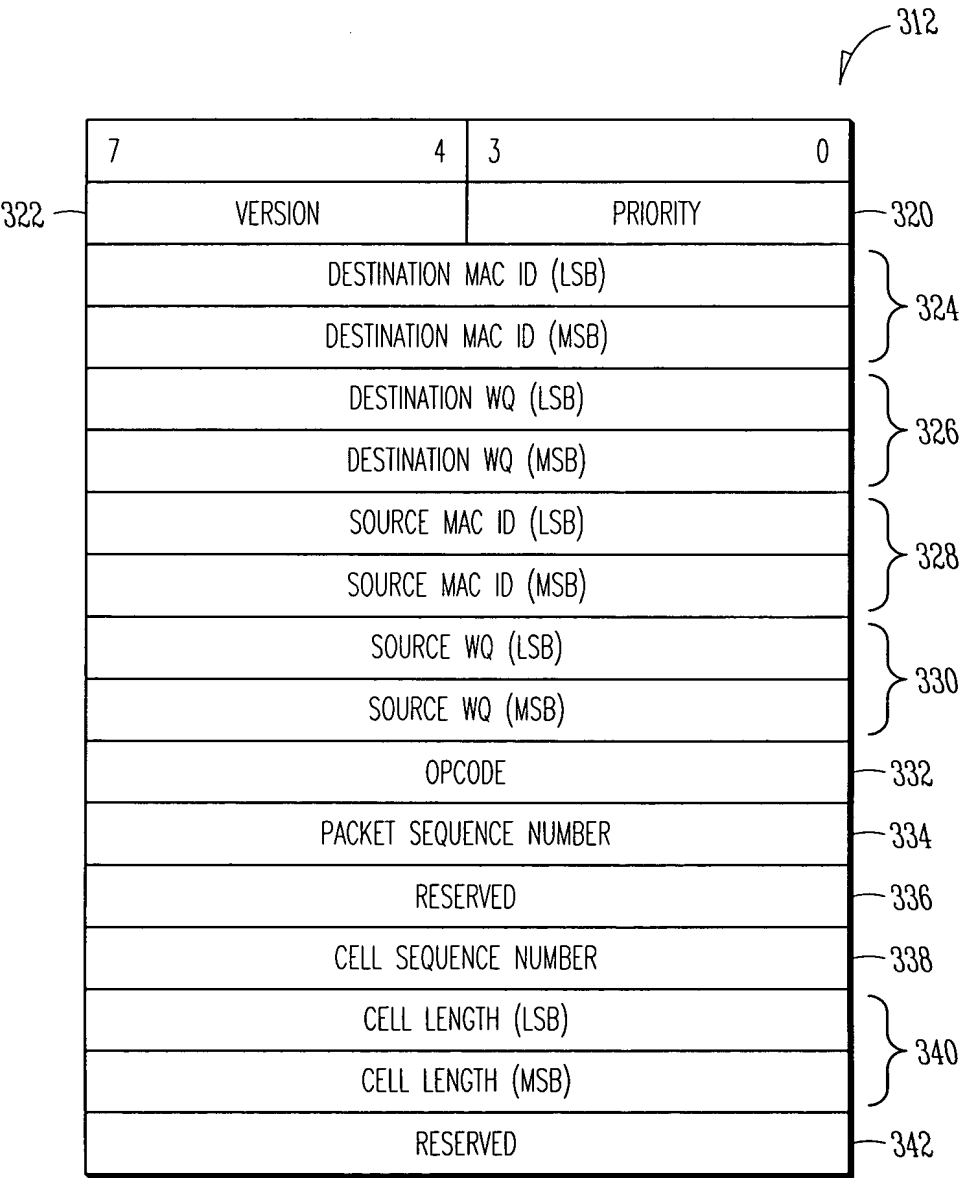


FIG. 3B

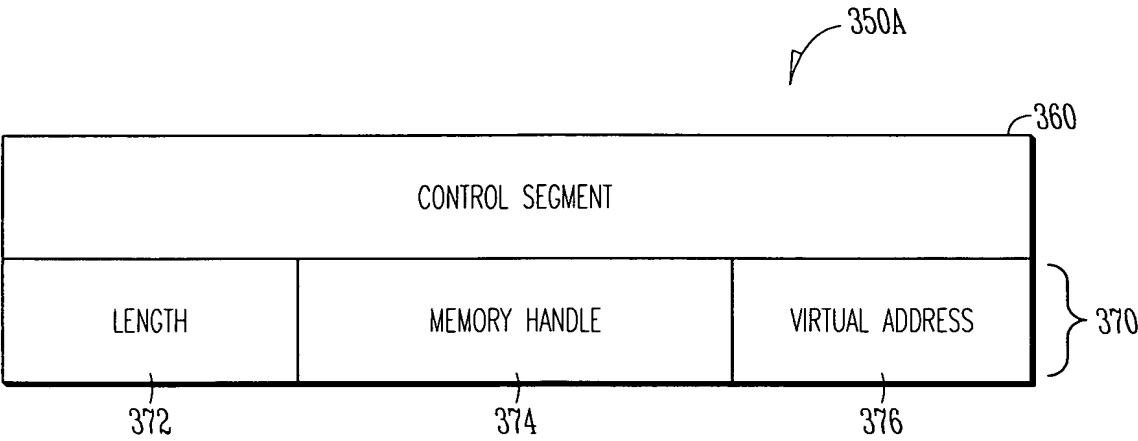


FIG. 3C

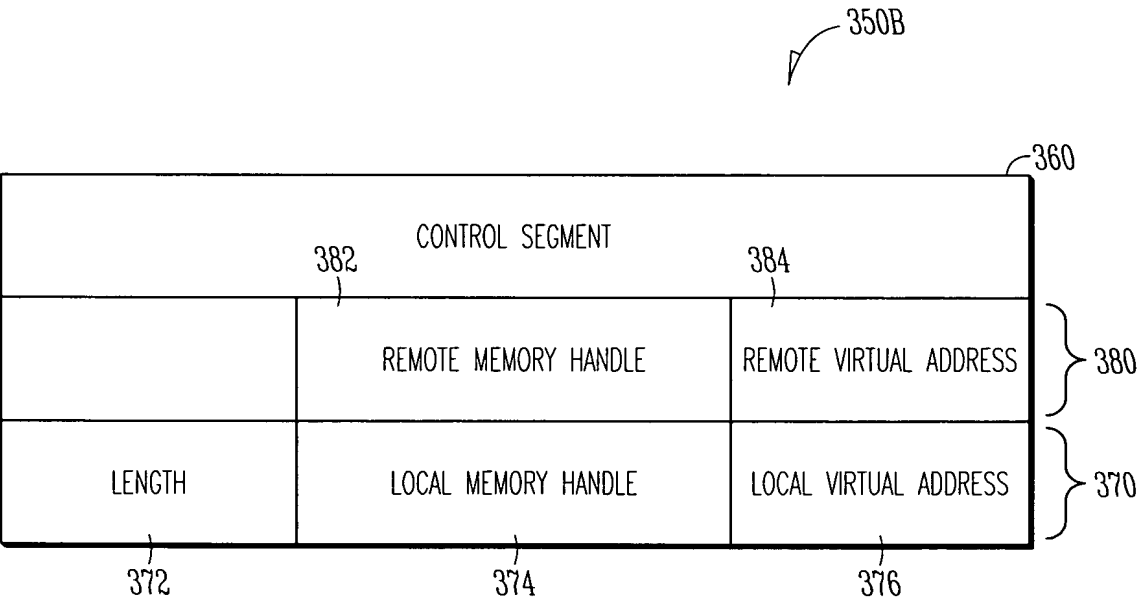


FIG. 3D

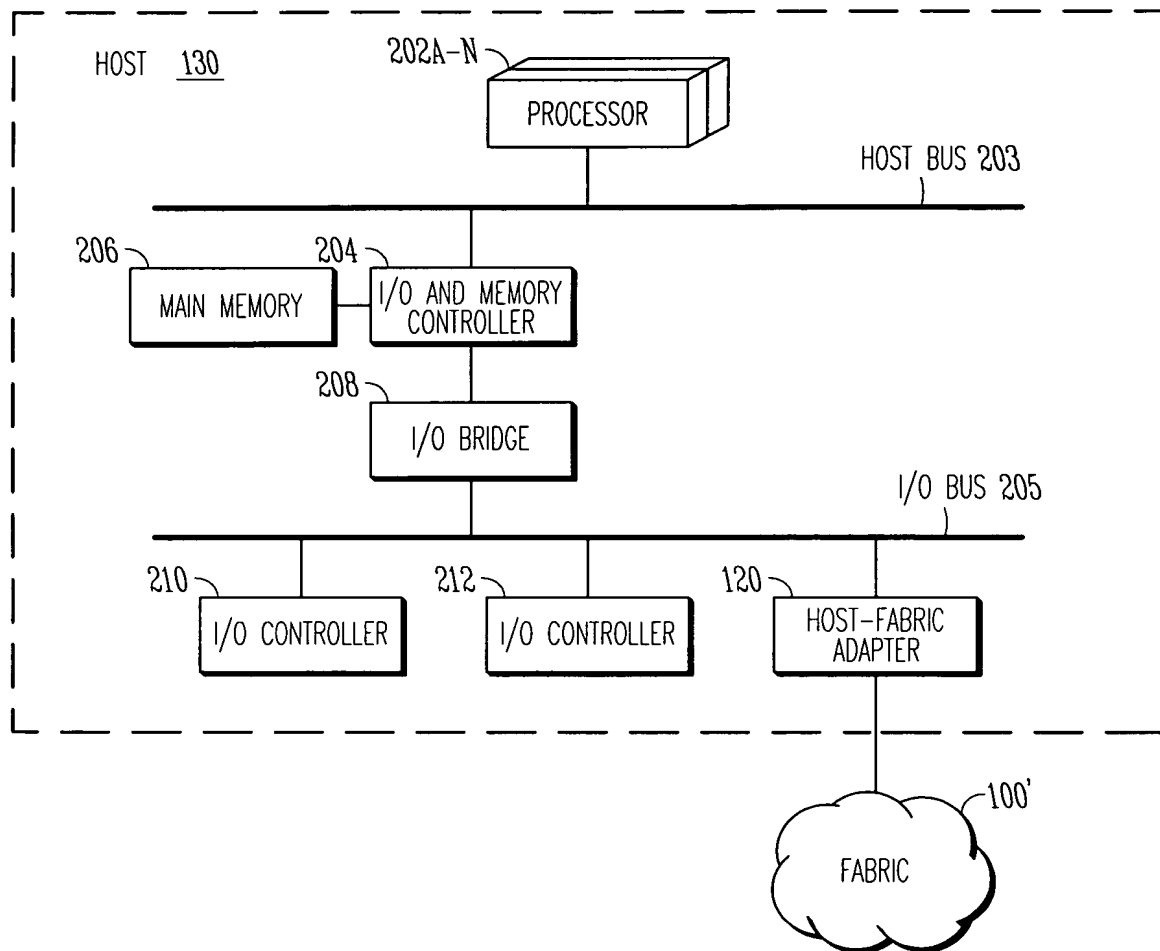


FIG. 4A

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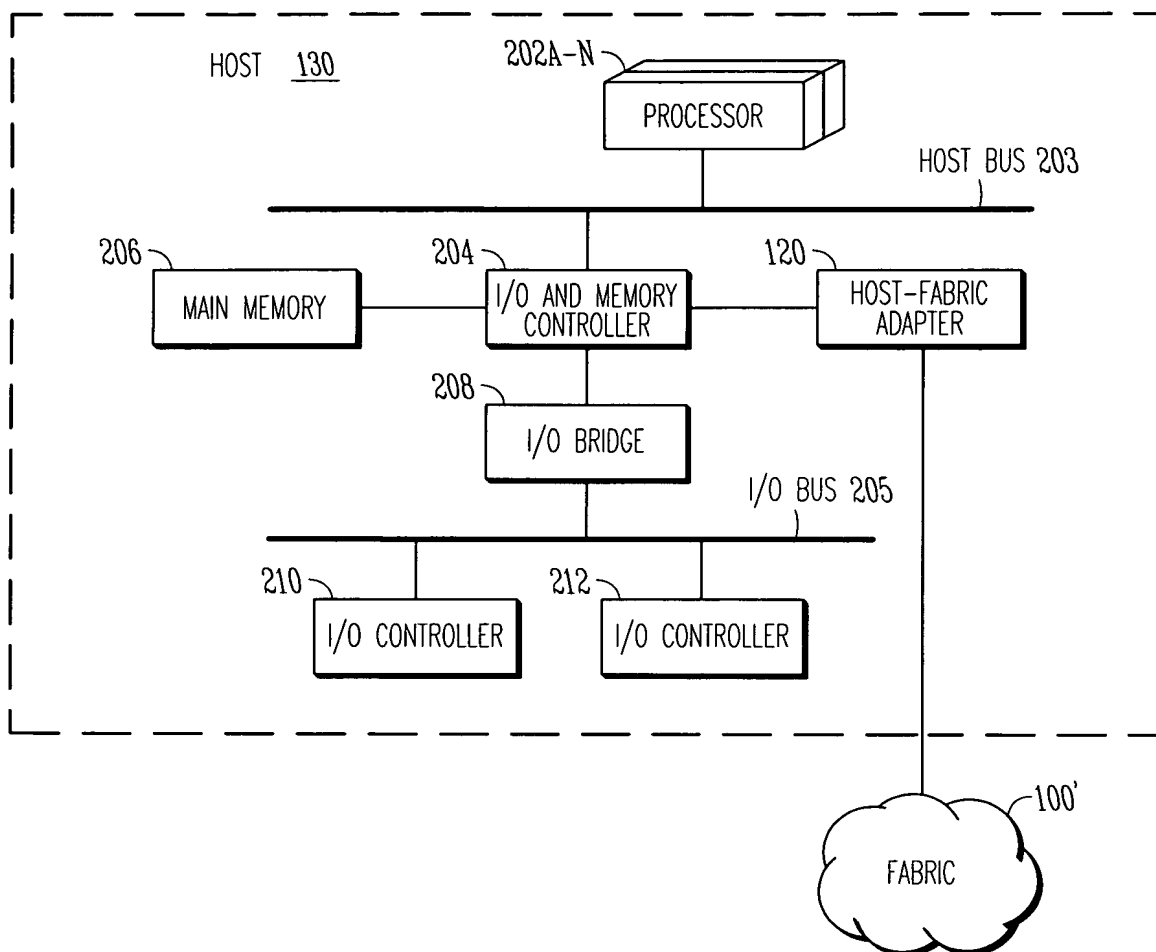
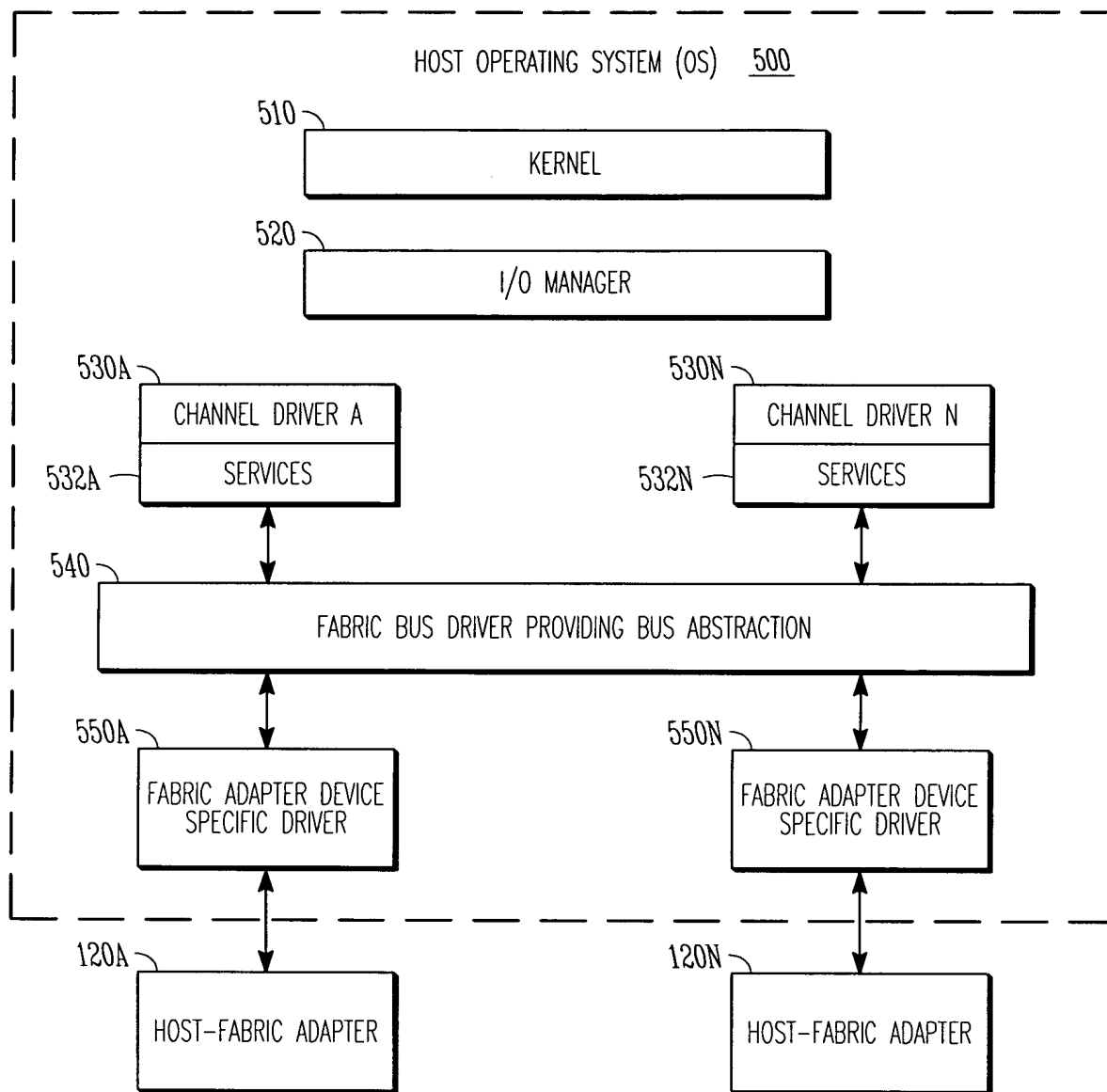


FIG. 4B

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EXAMPLE SOFTWARE DRIVER STACKS OF HOST SYSTEM

FIG. 5

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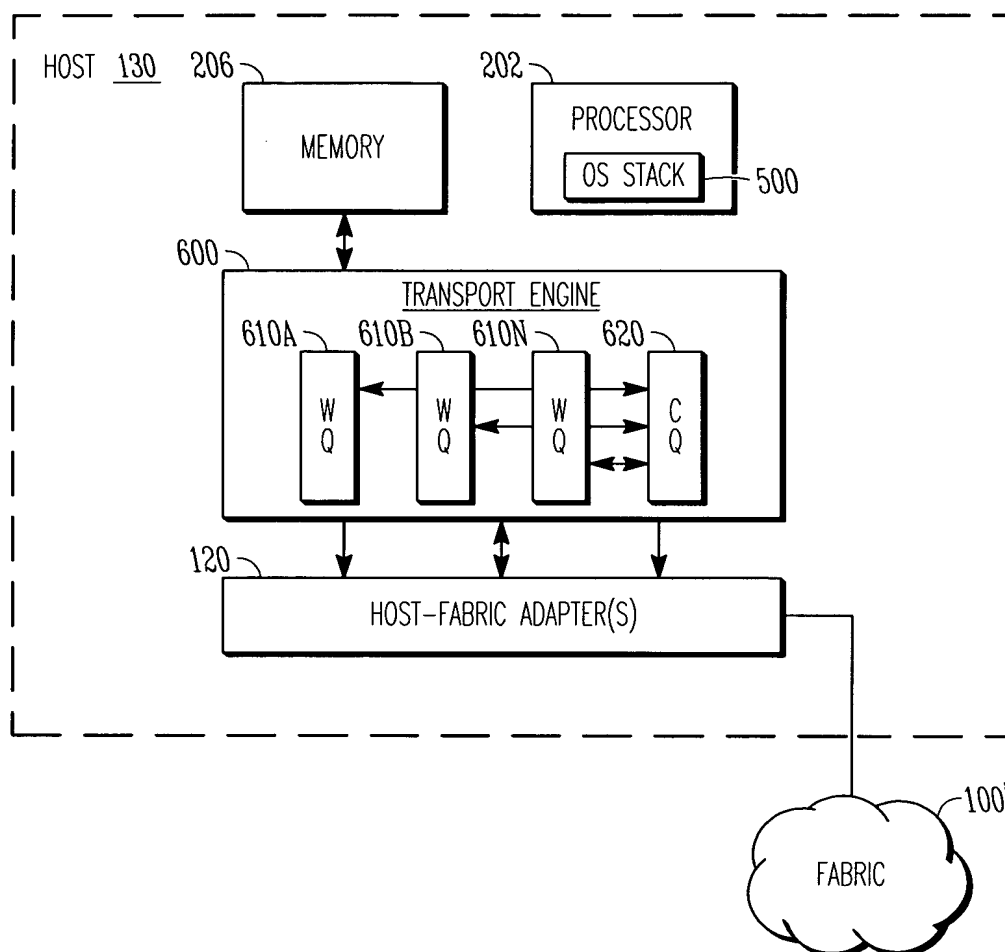


FIG. 6

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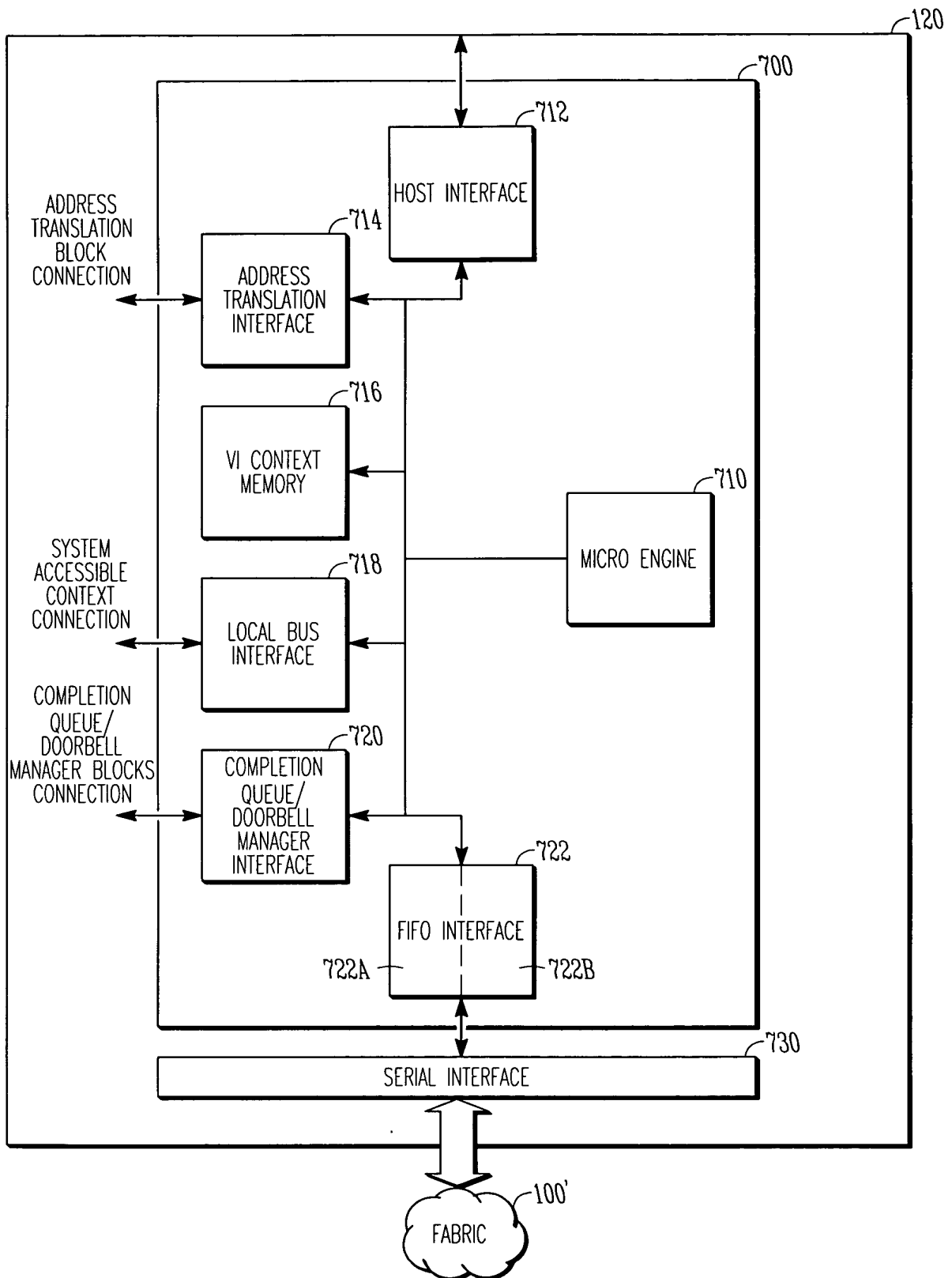


FIG. 7

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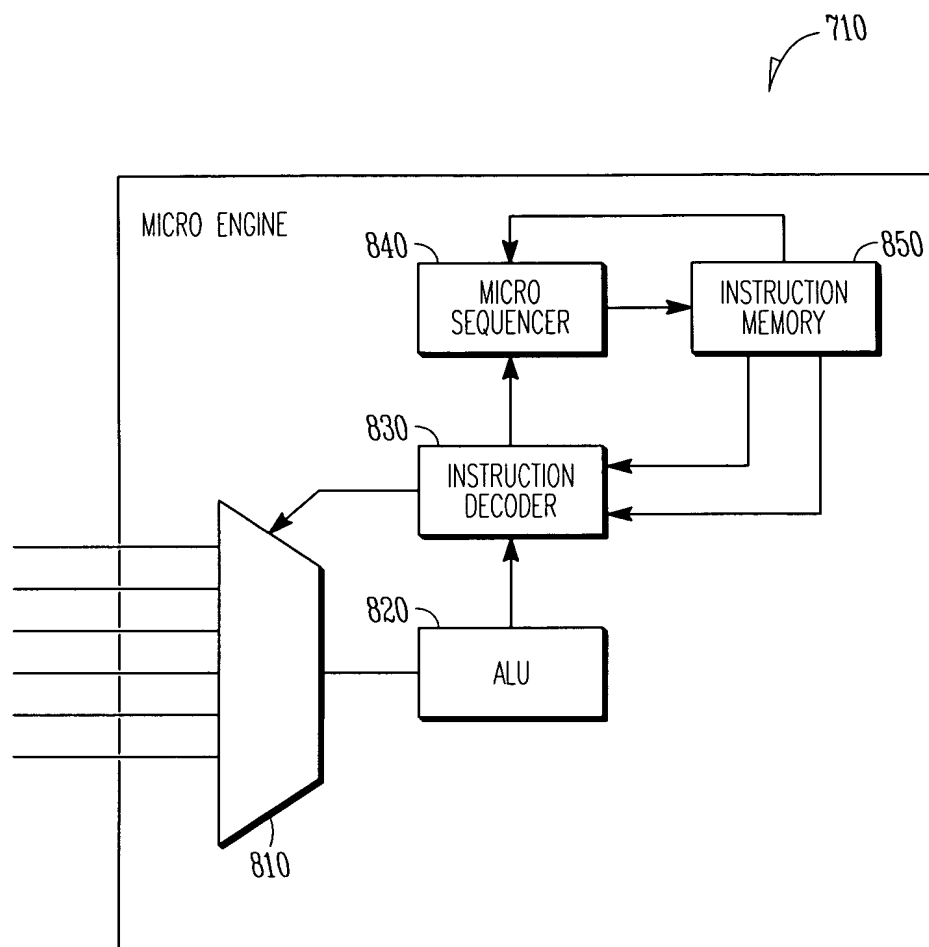


FIG. 8

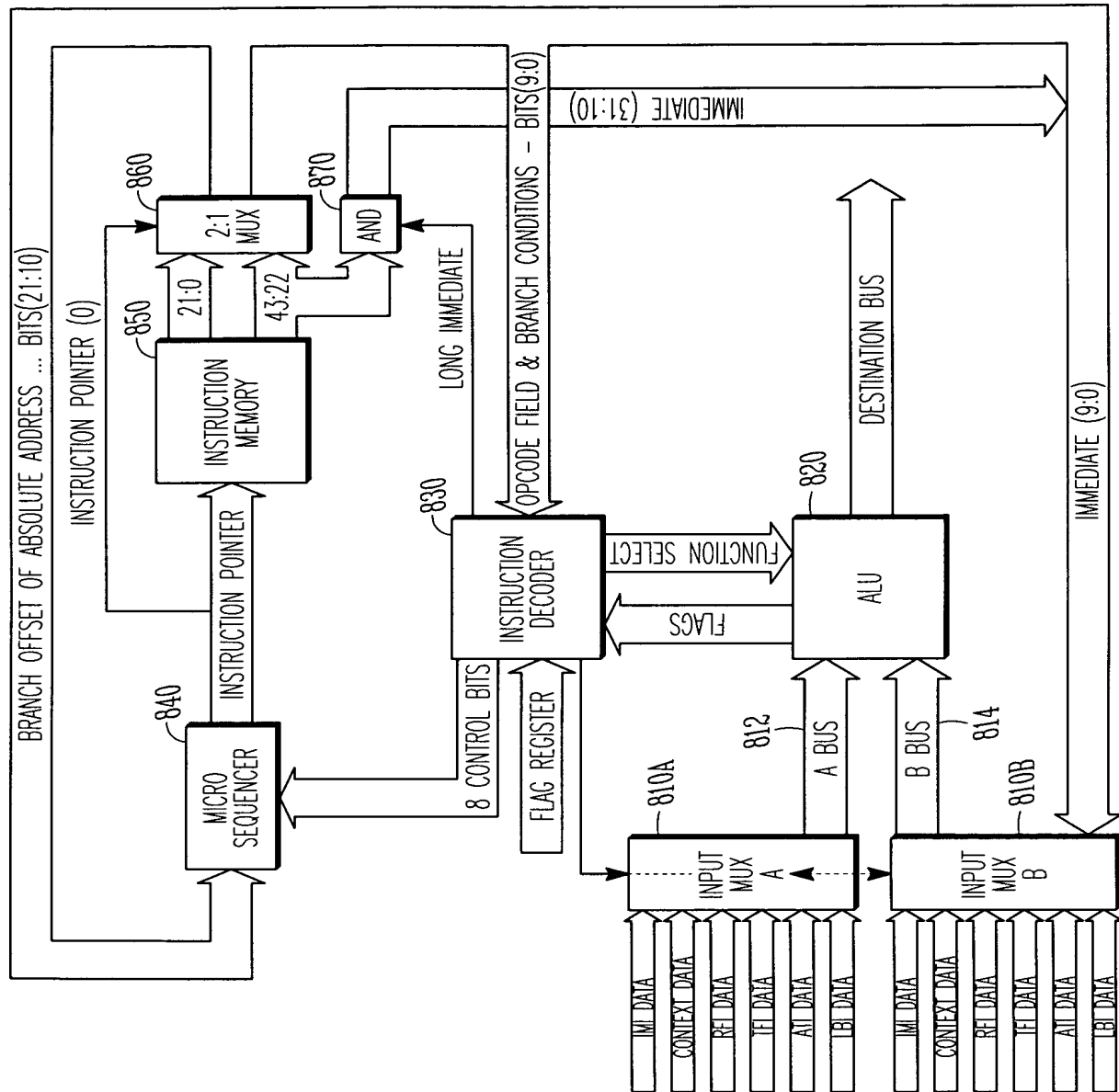


FIG. 9

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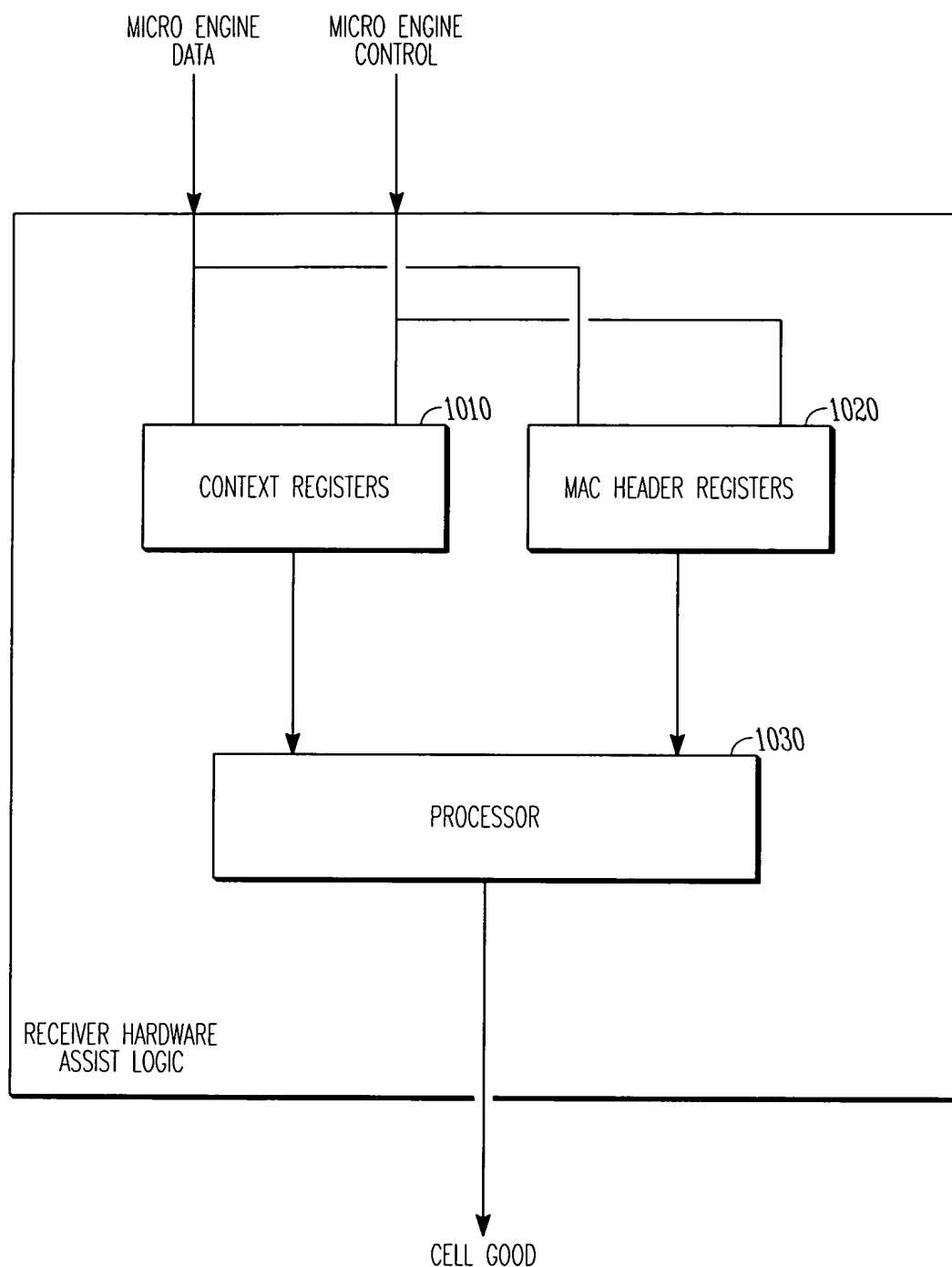


FIG. 10

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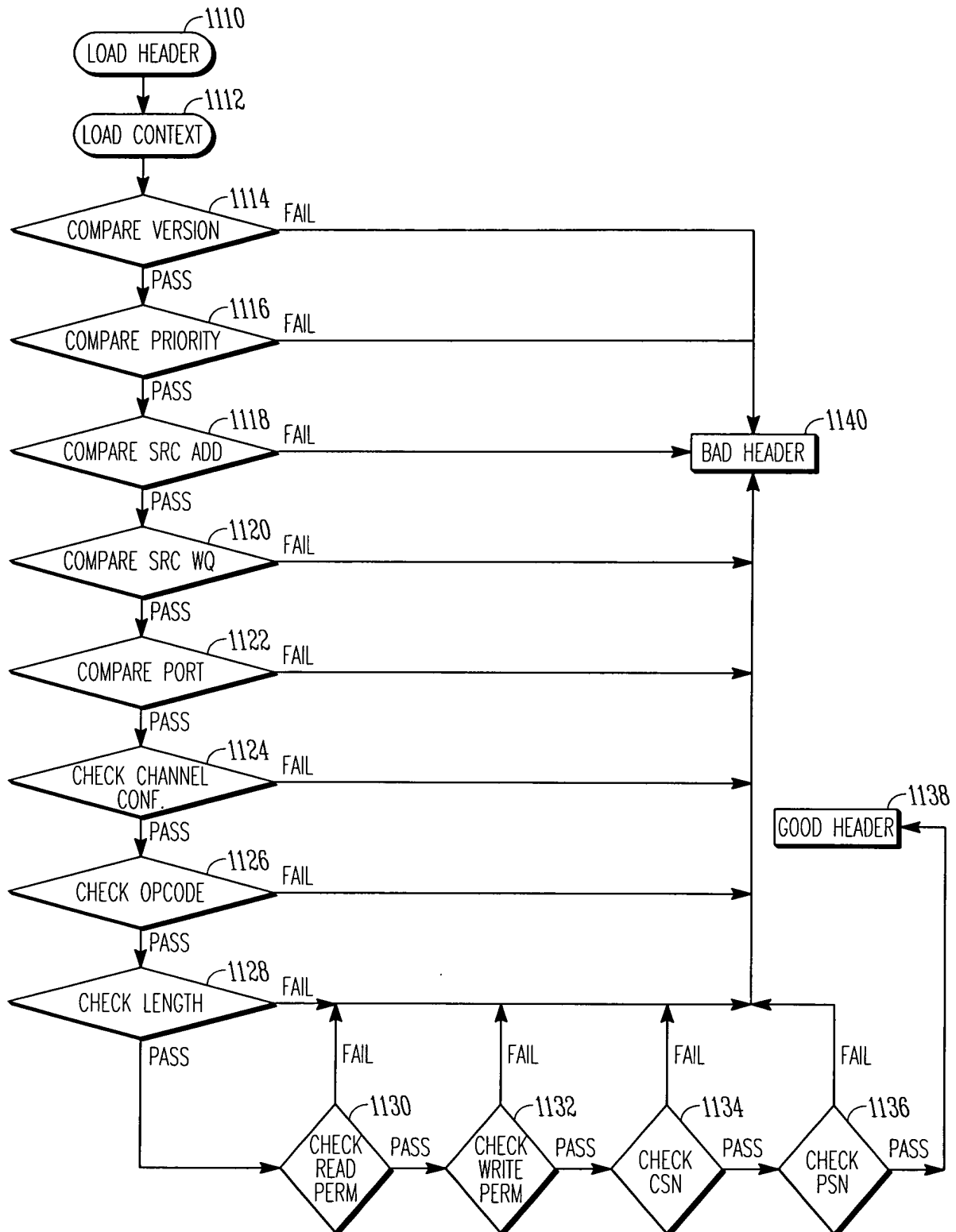


FIG. 11

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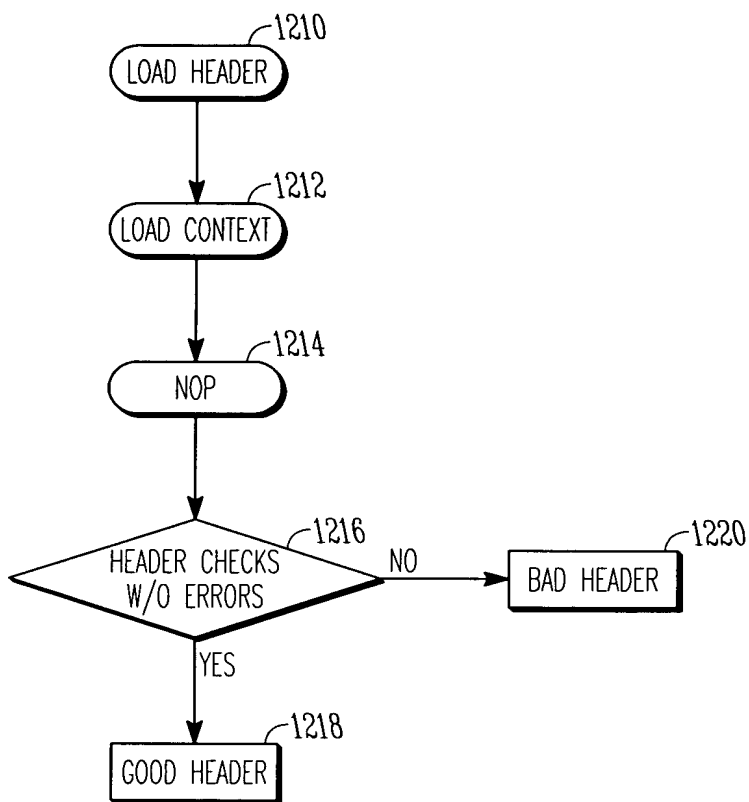


FIG. 12

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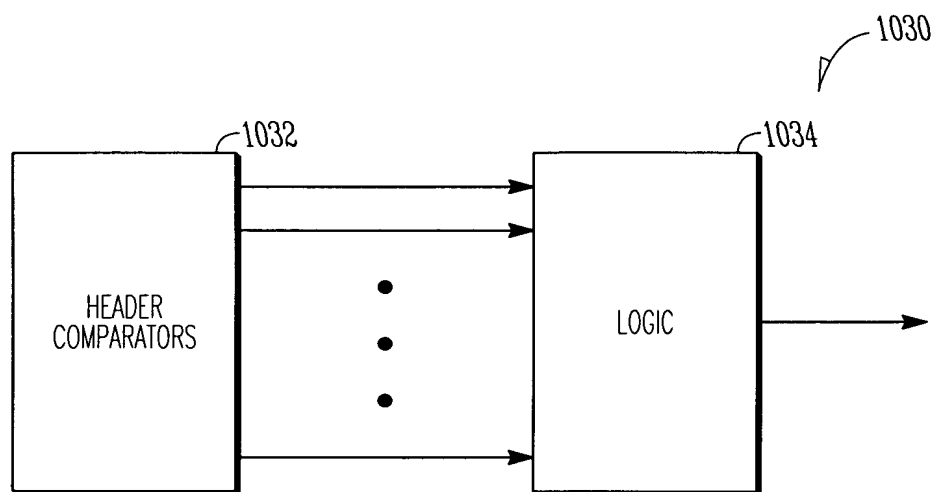


FIG. 13A

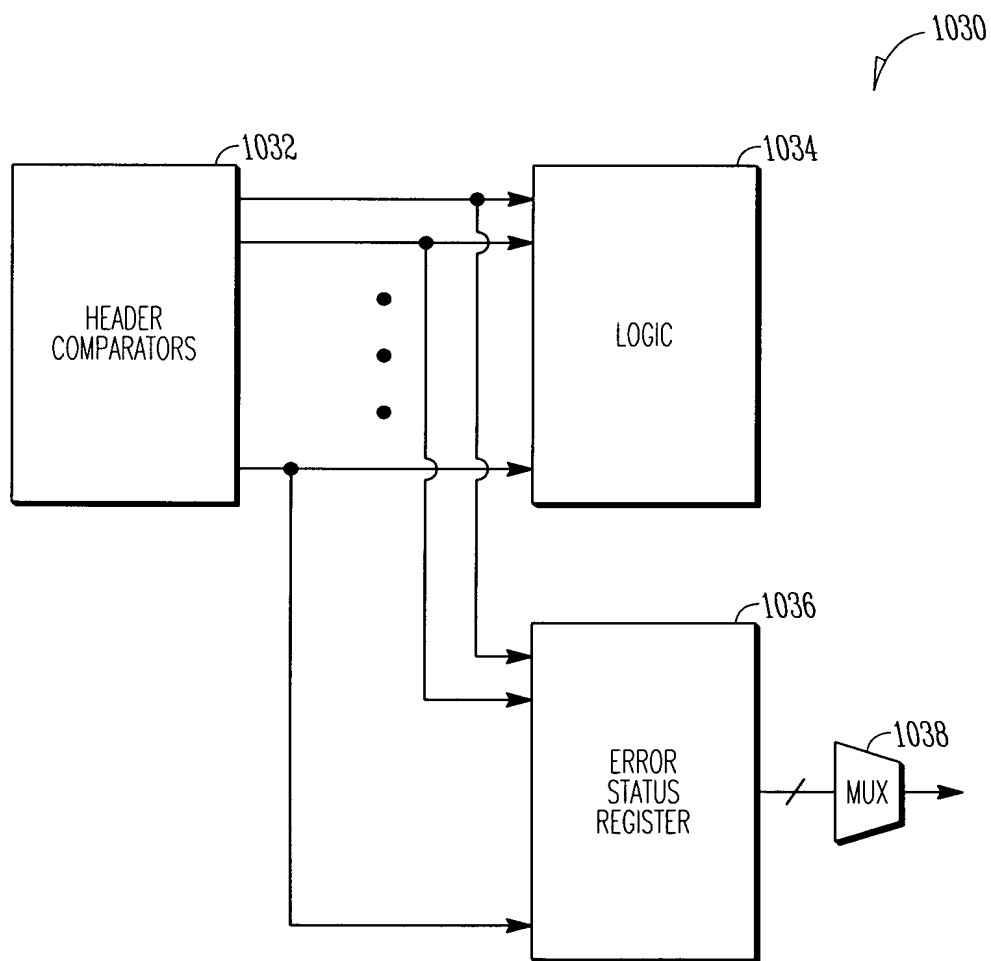


FIG. 13B

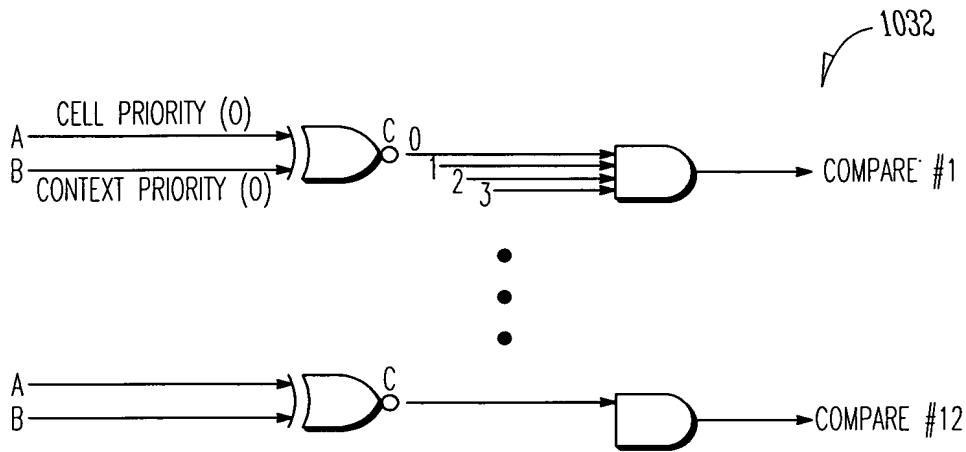


FIG. 14A

Diagram 1032 illustrates a logic circuit for comparing priorities. It shows a sequence of AND gates. The first gate takes inputs A (CELL PRIORITY (0)) and B (CONTEXT PRIORITY (0)) and produces output C (0). This output C (0) is then fed into a second AND gate along with other inputs (1, 2, 3) to produce COMPARE #1. This pattern repeats for other gates, with the final gate taking inputs A and B to produce COMPARE #12.

XNOR		
A	B	C
0	0	1
0	1	0
1	0	0
1	1	1

FIG. 14B

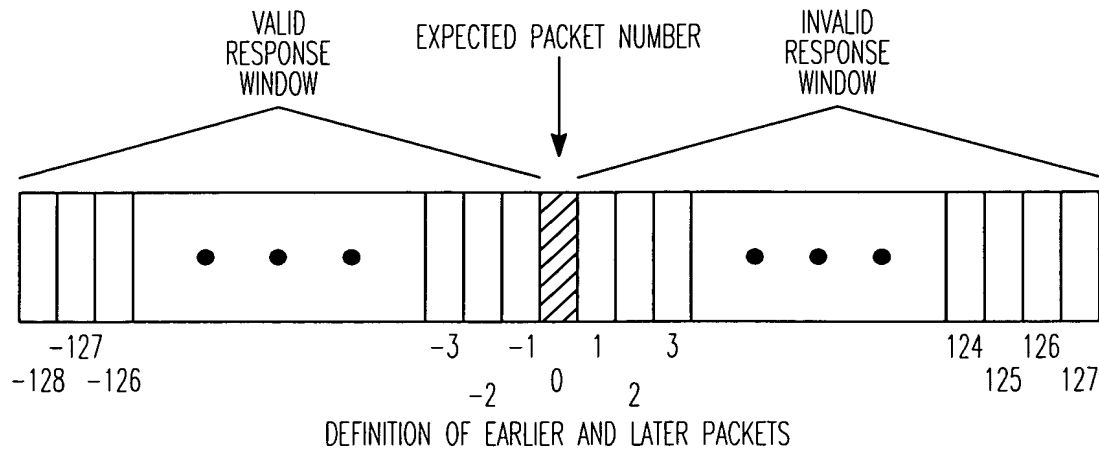


FIG. 15

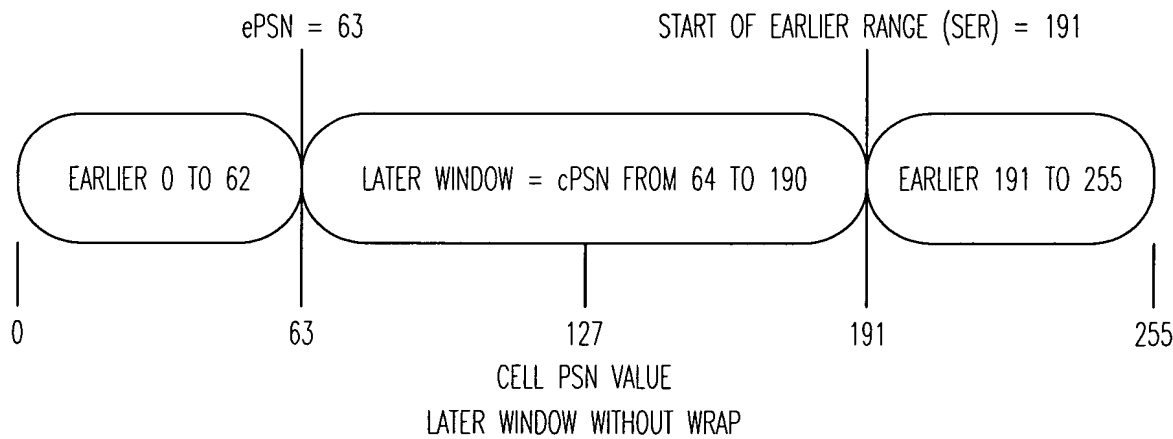


FIG. 16

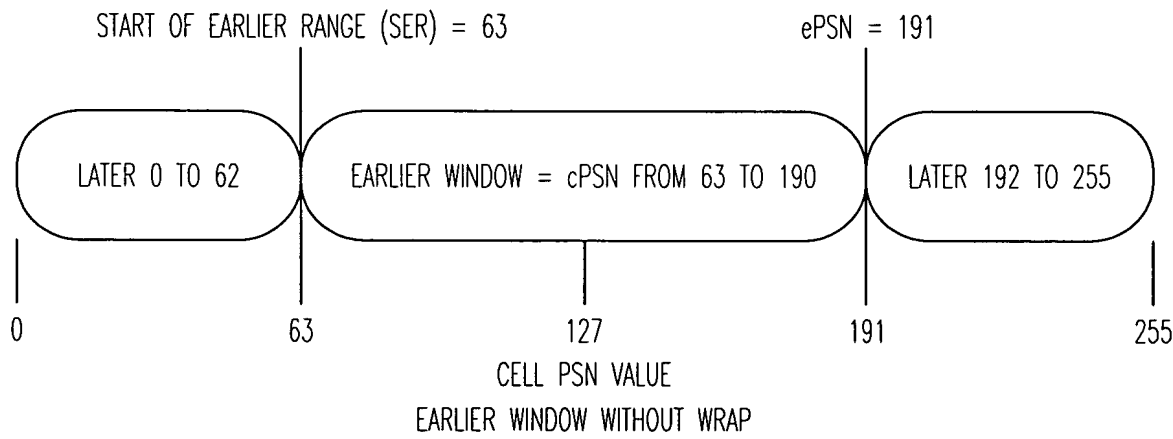


FIG. 17

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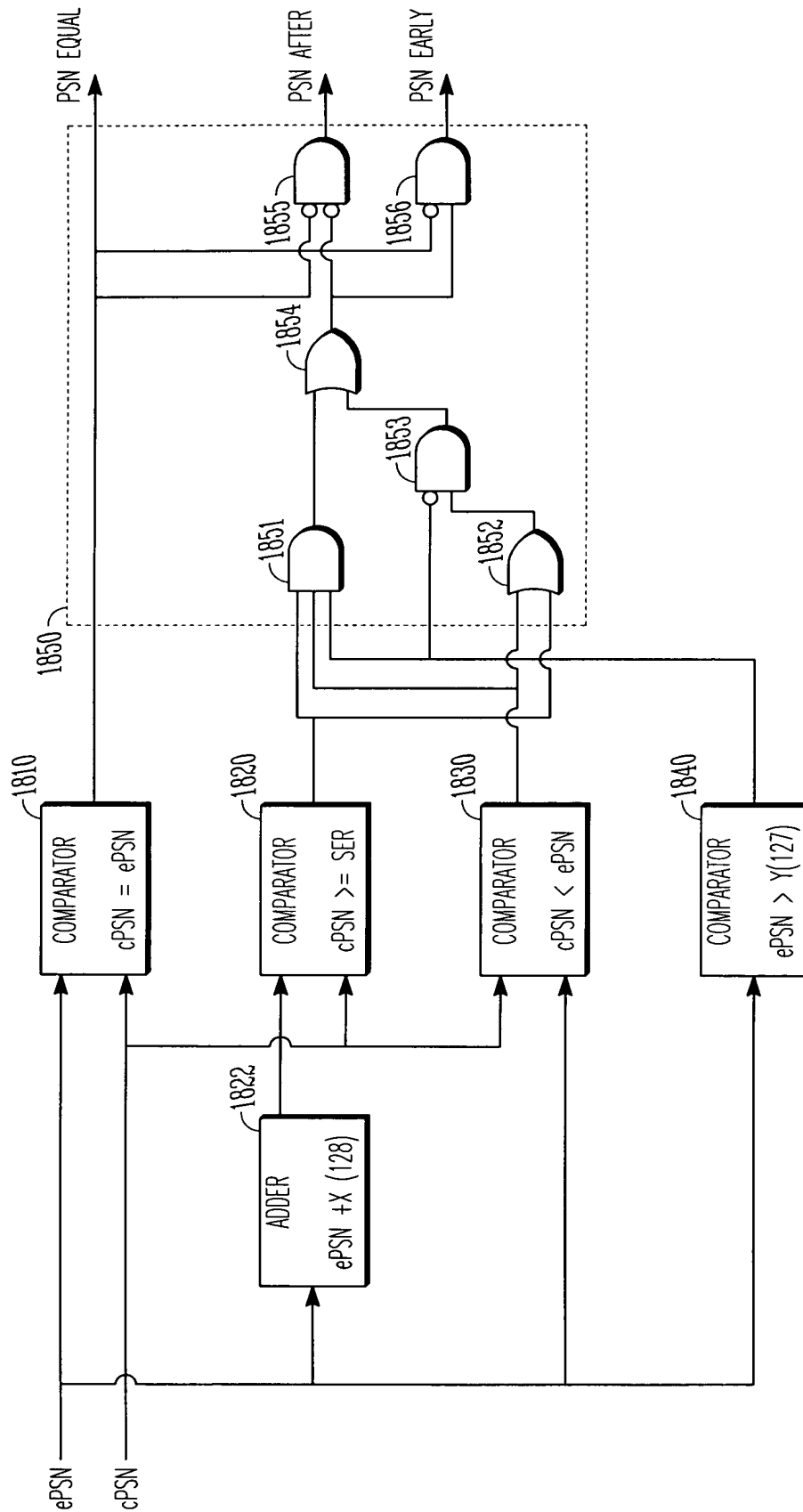


FIG. 18

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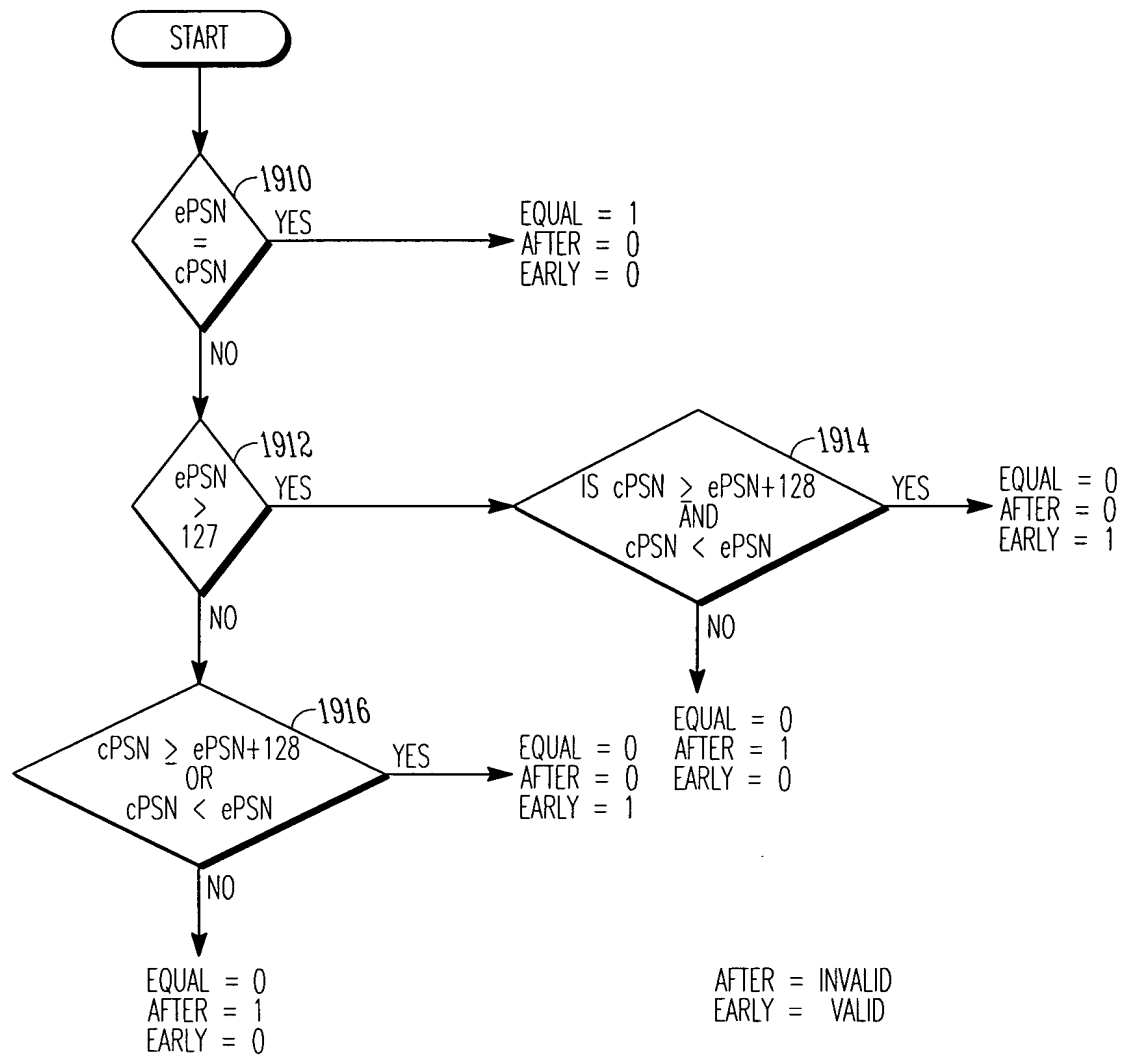


FIG. 19

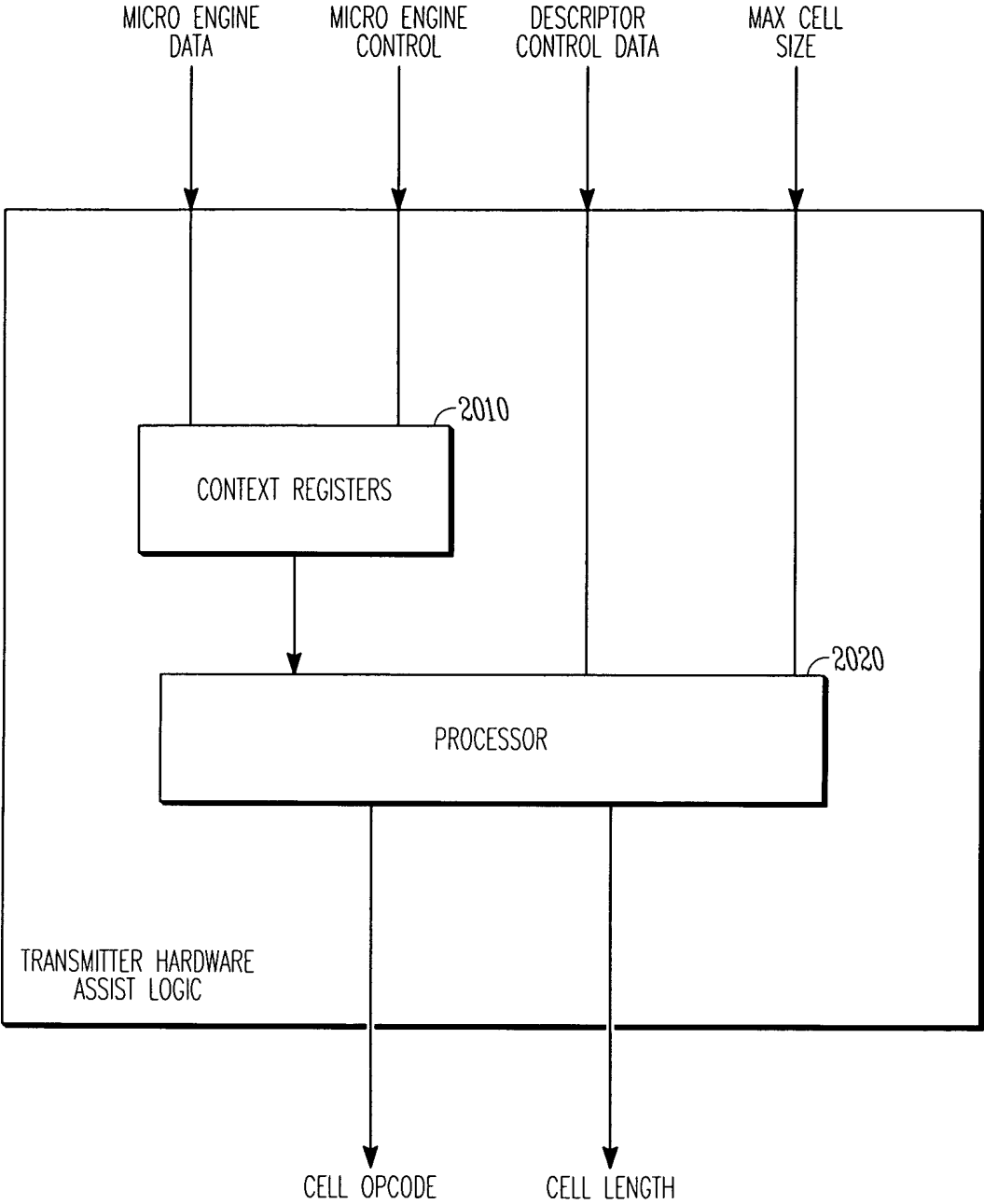


FIG. 20

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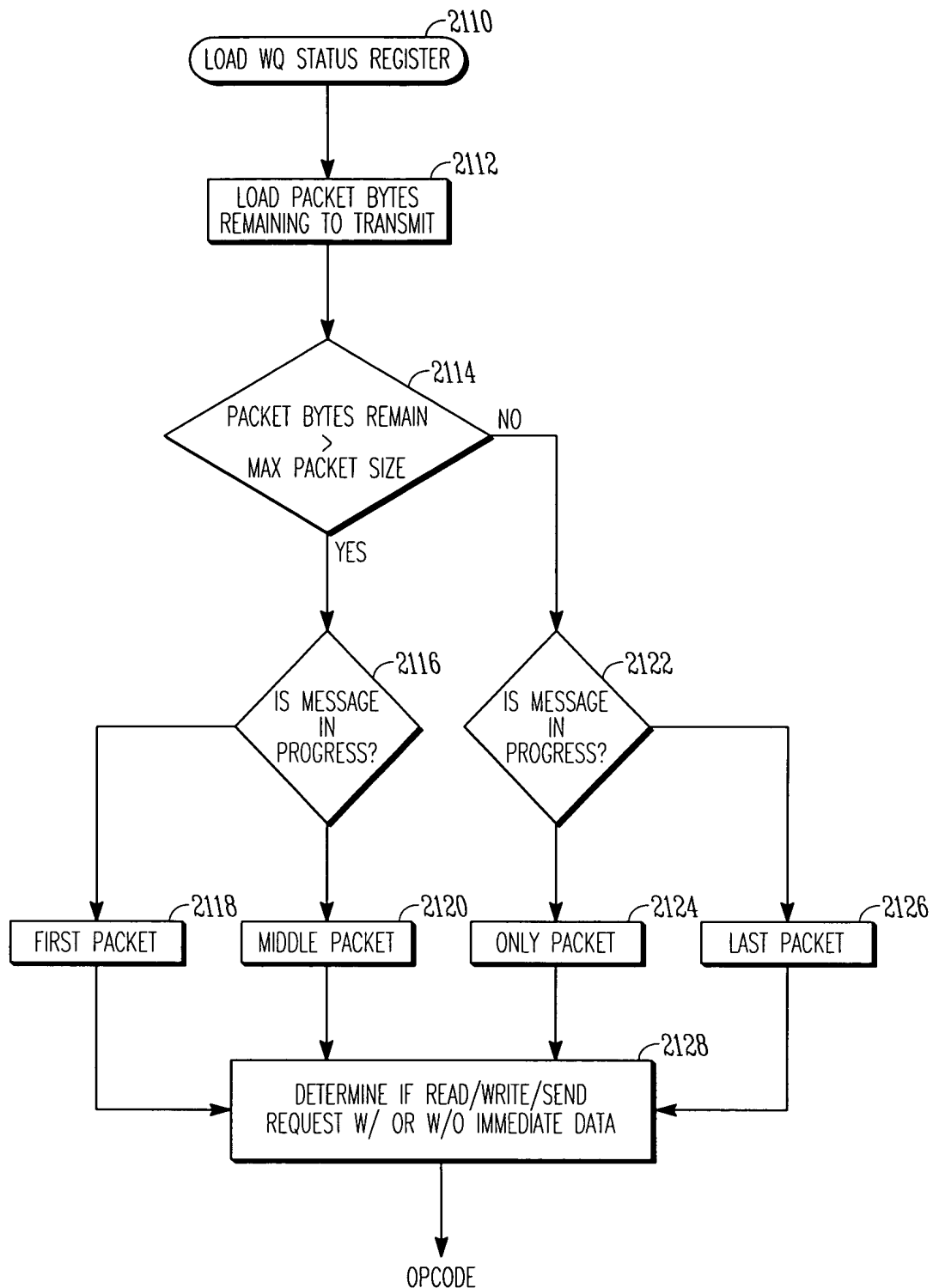


FIG. 21

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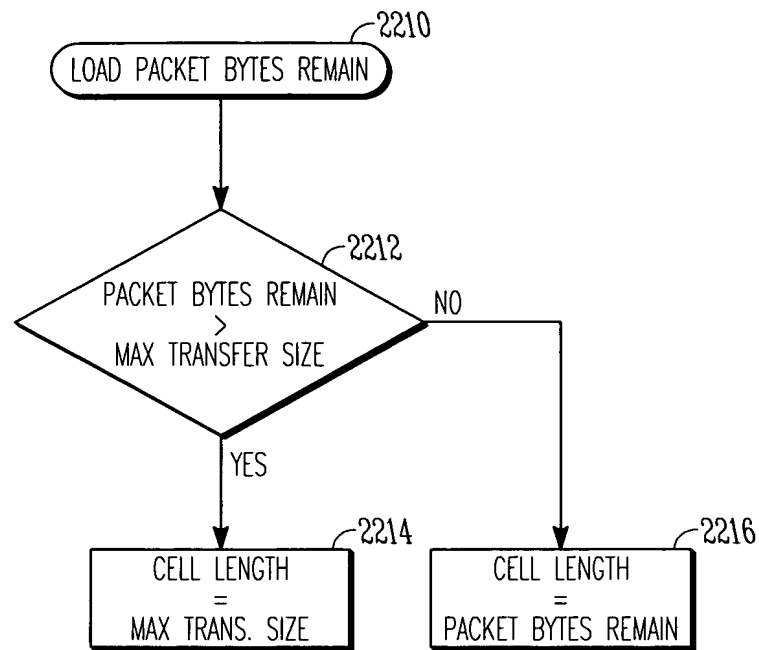


FIG. 22